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An MCT-Based Bit-Weight Extraction Technique for Embedded SAR ADC Testing and Calibration

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Abstract This paper presents a self-testing and calibration technique for the embedded successive approximation register (SAR) analog-to-digital converter (ADC) in system-on-chip (SoC) designs. We first proposed a low cost design-for-test (DfT) technique that estimates the SAR ADC performance before and after calibration by characterizing its digital-to-analog converter (DAC) capacitor weights (bit weights). Utilizing major carrier transition (MCT) testing, the required analog measurement range is only about 1 LSB; this significantly reduces test circuitry complexity. Then, we develop a fully-digital calibration technique that utilizes the extracted bit weights to correct the non-ideal I/O behavior induced by capacitor mismatch. Simulation results show that (1) the proposed testing technique achieves very high test accuracy even in the presence of large noise, and (2) the proposed calibration technique effectively improves both static and dynamic performances of the SAR ADC.

Keywords Successive approximation register ADC · ADC testing · ADC calibration · Capacitor mismatch · Major-carrier transition testing

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1 Introduction

The charge redistribution SAR ADC, which is known to scale well with CMOS technology and offers a good tradeoff among power, area, speed, and resolution [14], is widely used in modern SoC designs for communication, sensor, and multimedia applications. In these applications, the ADC bridges the real world analog signal and the powerful digital signal processing (DSP) resources; its performance dominates the system functionality and thus should be carefully tested and calibrated.

ADC testing is costly and time-consuming because it is mainly consisted of specification based functional testing which requires expensive mixed-signal test equipment and lengthy test time [2]. These problems become more challenging for embedded ADCs since the access to their inputs and outputs is no longer guaranteed. Several works have been proposed to address these problems. To reduce the need for expensive mixed-signal testers, [8] proposed a built-in-self-test (BIST) technique for on-chip ADC and DAC. This work embeds all the test circuitry into the chip and utilizes a delta-sigma modulation technique to generate the test stimuli. However, the required test accuracy may be unattainable. To reduce the test time, [6, 7] proposed a selective code measurement technique for SAR ADC. It utilizes high-precision piecewise linear ramps to measure a set of properly selected code widths. From the results, the ADC linearity can be derived. However, this technique is incapable of handling the missing code issue and generating the required ramp signal on-chip is impractical. Huang et al. [9] proposed to test the SAR ADC by characterizing the capacitor DAC (CDAC). With MCT testing, the required test time and

test circuitry complexity can be significantly reduced, and all the missing codes can be successfully identified. However, it is limited to single-ended applications.

The performance of charge redistribution SAR ADC is mainly limited by the matching accuracy of the CDAC. Without proper trimming or calibration, the resolution of SAR ADC is generally bounded to 6-8 bits. Over the years, several works have been developed to improve the SAR ADC performance. One straightforward approach is to use large sampling capacitors to meet the matching requirement for the desired ADC resolution. However, the required capacitor size is usually much greater than the kT/C limit; this can cause severe area overhead and power consumption [10]. Ohnhaeuser et al. [16] calibrates the SAR ADC nonlinearity by injecting a compensation voltage into the CDAC during each bit decision. It requires an extra bandgap reference circuit, a high-gain operational amplifier (OPAMP), and a complex resister array for generating the needed compensation signal; this can significantly increase the circuit design complexity. Liu et al. [11, 12] utilize an adaptive digital filter (ADF) to calibrate the ADC raw codes. With the assistance of a slow but accurate reference ADC, the coefficients in the ADF are dynamically updated by the least-mean-square (LMS) algorithm to track the PVT (process, supply voltage, temperature) variations. However, the reference ADC usually incurs significant area overhead and should be pre-calibrated to ensure the achievable calibration accuracy [18]. Liu et al. [13] proposed another adaptive trimming technique that is based on input signal perturbation; it does not require an additional reference ADC but the conversion speed is halved. In general, these adaptive calibration techniques are effective for correcting the errors induced by the capacitor mismatch. However, they usually require lengthy calibration time for the results to converge. As the production testing should be conducted after calibration, these techniques can substantially increase the test cost [3]. There are also techniques proposed to use additional comparisons to tolerate the noise induced conversion error [4, 5]. Nevertheless, these extra comparisons are themselves very vulnerable to noise because the two inputs to the comparator become very close at the end of the conversion.

This work presents an MCT-based bit-weight extraction technique for testing and calibrating the embedded SAR ADC. First, we proposed a low-cost DfT technique that extracts the CDAC bit weights by measuring MCTs. Here, the MCTs are generated by a modified SAR operation, and measured by (1) the SAR ADC comparator and (2) an auxiliary DfT DAC (d-DAC) that couples to the dummy capacitor in the CDAC. From the results, the individual bit weights can be derived and the ADC I/O behavior can be predicted for performance analysis. Then, to improve the ADC linearity, we propose a fully-digital calibration technique that can be integrated into the proposed testing scheme; it employs the extracted bit weights to correct the non-ideal I/O behavior caused by capacitor mismatch.

The contributions and advantages of this work are as follows.

1. The full scale range (FSR) of the MCT measurement is small—close to 1 LSB; this drastically simplifies the d-DAC implementation.
2. The test control signals and the test responses are all digital. Therefore, the on-chip digital resources can be used for analyzing the test results and thus estimating the ADC performance; this substantially lowers the test cost.
3. The proposed testing technique is capable of estimating the SAR ADC performance both before and after calibration. The pre-calibration results can be used to determine whether the SAR ADC needs calibration or not, and the post-calibration results can be used to make the go/no-go decision.
4. The proposed calibration technique is fully-digital and requires no SAR ADC modification. All the required computation can be executed from the on-chip DSP/CPU as a software routine; this significantly reduces the incurred circuit design complexity and area overhead.

The rest of this paper is organized as follows. In Section 2, the basic architecture, operation principle, and error sources of the SAR ADC are reviewed. Section 3 discusses the linear histogram testing as well as the MCT testing. In Section 4, the proposed technique is described in details, including the MCT measurement, bit weight extraction algorithm, and the testing/calibration procedures. Simulation results are given in Section 5, and we conclude this paper in Section 6.

2 SAR ADC Review

2.1 Basic Architecture

Shown in Fig. 1 is the basic architecture of an N-bit SAR ADC; it consists of an analog comparator, a SAR control logic, and a binary-weighted CDAC where $C_i = 2^i \cdot C_{\text{dummy}}$ for $i = 0$ to $N-1$. This figure only shows a single-ended design for simplicity, but all the results are applicable to fully-differential implementation.

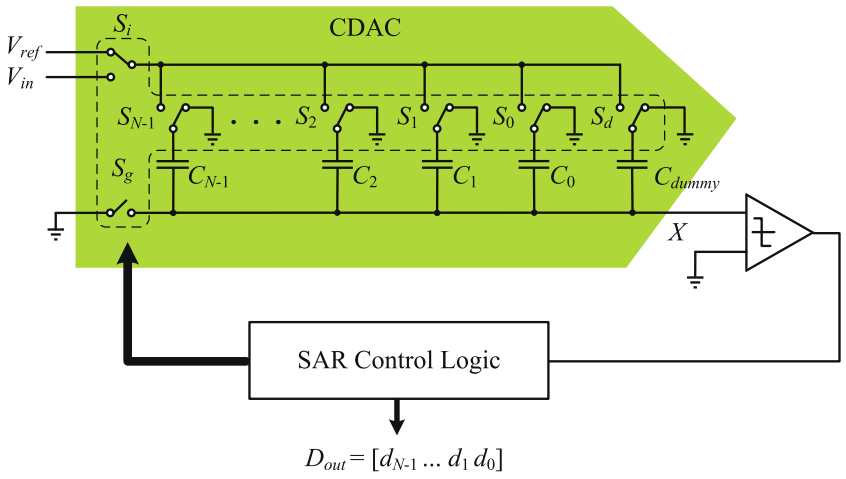

Fig. 1 The SAR ADC architecture

The analog-to-digital (A/D) conversion of SAR ADC is accomplished by a sequence of three operations [15].

1. **Sample.** By connecting the capacitor top plates to the analog input and closing the grounding switch S_g, the SAR ADC tracks V_{in}.
2. **Hold.** By opening S_g and connecting the capacitor top plates to ground, the voltage at node X, denoted by V_X, becomes $-V_{\text{in}}$.
3. **Charge Redistribution.** To resolve MSB (the most significant bit), C_{N-1} top plate is connected to V_{ref}. Charge redistribution forces V_X to be as follows.

$$V_X = -V_{\text{in}} + \frac{C_{N-1}}{C_{\text{total}}} \cdot V_{\text{ref}} = -V_{\text{in}} + \frac{1}{2} V_{\text{ref}} \tag{1}$$

where $C_{\text{total}} = C_{\text{dummy}} + \sum_{i=0}^{N-1} C_i = 2^n \cdot C_{\text{dummy}}$. If $V_X < 0$, we have $d_{N-1} = 1$; otherwise, d_{N-1} should be 0 and the top plate of C_{N-1} is connected to ground. This process is repeated N times until d_0 is resolved.

Assume that the comparator is ideal and the CDAC is monotonic. (The non-monotonic cases will be discussed later.) According to the SAR operation principle, the SAR ADC output code is D if the input voltage V_{in} is between the CDAC outputs of codes D and $D+1$. Thus, the code transition level (V_{TL}), i.e., the lower code edge, of $D = d_{N-1} \ldots d_1 d_0$ can be derived as

$$V_{\text{TL}}(d_{N-1} \ldots d_1 d_0) = \frac{\sum_{i=0}^{N-1} d_i \cdot C_i}{C_{\text{total}}} \cdot V_{\text{ref}} \tag{2}$$

2.2 Error Sources

Among the various SAR ADC error sources, the comparator offset and the CDAC capacitor mismatch cause the most significant non-ideal I/O behavior.

2.2.1 Comparator Offset

The comparator offset causes a global shift to the SAR ADC transfer curve and thus decreases the ADC dynamic range. Typically, auto-zeroing and correlated double sampling (CDS) techniques are employed to deal with the offset errors.

Note that, for the conventional SAR ADC, the input-dependent comparator offset is less an issue and does not affect the overall linearity [11]. This is mainly because the two inputs to the comparator always converge to the common mode voltage (analog ground) at the end of each conversion.

2.2.2 Capacitor Mismatch

In the presence of capacitor mismatch, the ADC I/O transfer curve may exhibit missing-decision-levels (MDLs) or missing codes (a.k.a. missing transition levels, MTLs).

Before describing the capacitor mismatch effects, let's define $\hat{\mathcal{M}}_i$ as the set of codes for which $(d_i d_{i-1} \ldots d_0)_2 = 2^i$, as shown in Eq. 3.

$$d_j = \begin{cases} \text{don't care} & \text{if } j > i \\ 1 & \text{if } j = i \\ 0 & \text{if } j < i \end{cases} \tag{3}$$

According to the definition, $|\hat{\mathcal{M}}_i| = 2^{N-i-1}$. Furthermore, let's denote the codes in $\hat{\mathcal{M}}_i$ by $\mu_{i,k}$ where the index k is the value represented by $d_{N-1} d_{N-2} \ldots d_{i+1}$. For example, if $N = 10$, we have $\hat{\mathcal{M}}_8 = \{\mu_{8,0}, \mu_{8,1}\}$ where $\mu_{8,0} = 0\underline{1}00000000$, and $\mu_{8,1} = 1\underline{1}00000000$ (the underlined bits are the eighth bits). As will be seen later, $\hat{\mathcal{M}}_i$ contains codes where nonlinearity due to capacitor mismatch associated with bit i occurs or can be observed.

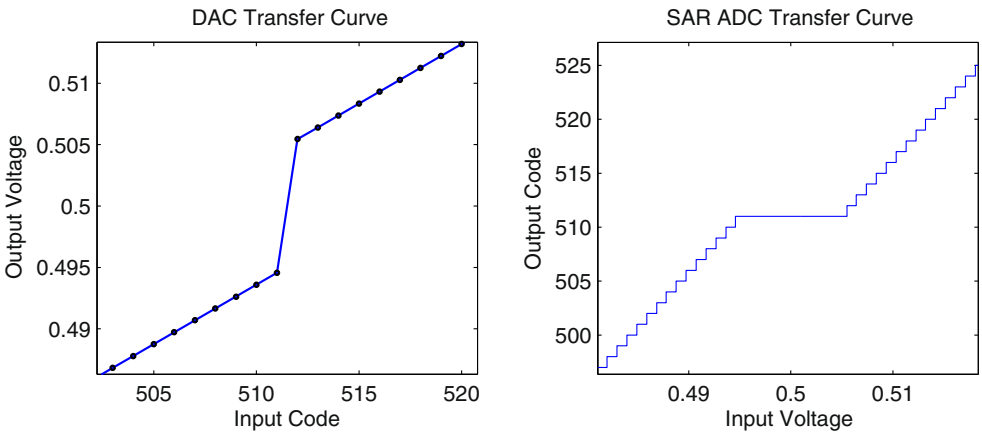

Fig. 2 The missing decision level in 10-bit SAR ADC

MDL occurs when $C_i > \sum_{j=0}^{i-1} C_j + C_{\text{dummy}}$; the result is excessively large code widths for codes that equal $\mu_{i,k} - 1$ for some k. Figure 2 shows a 10-bit SAR ADC with MDL error. Here, C_9 is larger than its ideal value by 2 % while the other capacitors are ideal; this causes a voltage jump from code 511 to 512 in the CDAC transfer curve (left-hand side plot) and thus results in MDL at code 511, i.e., $\mu_{9,0} - 1$, in the SAR ADC transfer curve (right-hand side plot).

Missing codes, on the other hand, are due to $C_i < \sum_{j=0}^{i-1} C_j$. In such cases, the CDAC I/O transfer curve becomes non-monotonic for codes in $\hat{\mathcal{M}}_i$. Because the SAR principle resolves more significant bits prior to less significant bits, the non-monotonicity causes some CDAC outputs to be never compared to and the corresponding codes become missing codes. For example, the left-hand side plot in Fig. 3 shows the transfer curve of a 10-bit CDAC for which $C_9 < \sum_{j=0}^{8} C_j$; it becomes non-monotonic at output transition from code 511 to 512, i.e., $\mu_{9,0}$. In this example, code 502 to 511 will never be compared to (because the corresponding CDAC outputs are greater than that of code 512) and become missing codes (right-hand side plot of Fig. 3).

Note that MDL incurs information loss and cannot be fixed by external calibration. Conventionally, MDL is avoided by adopting the sub-radix-2 conversion architecture in which the conversion radix $\alpha = C_i/C_{i-1}$ is set to be less than two. Although effective, the sub-radix-2 conversion adversely increases the number of missing codes and thus decreases the achievable resolution. Fortunately, the missing codes can be easily corrected externally in the digital domain and the overall resolution can be maintained by adding a few redundant bits [11–13].

It should also be noted that, because capacitor mismatch causes the code transition levels to deviate from their ideal values, the resolved ADC raw code may not be the "true" digital representation of the input voltage. According to Eq. 2, the "true" output code can be derived from the ADC raw code if the capacitor weights, or more precisely, the bit weights, are known; this forms the basis of the proposed technique.

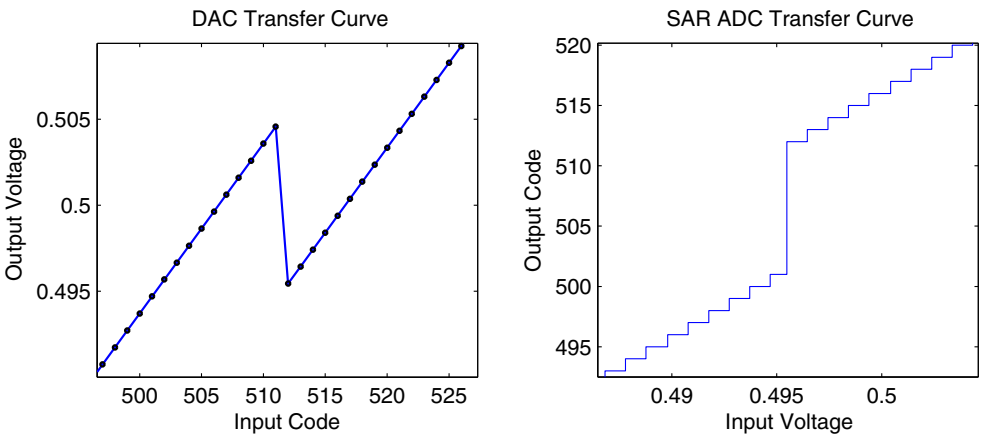

Fig. 3 The missing codes in 10-bit SAR ADC

3 SAR ADC Linearity Testing

In this section, we first introduce the linear histogram testing and the performance metrics that are commonly used for characterizing the ADC linearity. Then, we discuss how to estimate the SAR ADC performance by MCT testing.

3.1 ADC Linear Histogram Testing

The ADC linearity is usually characterized by the linear histogram testing; a linear ramp of which the linearity is better than the ADC by at least 3 bits is applied and the ADC output codes are collected. Let $H(i)$ be the number of occurrences of output code i. The average code hits, which corresponds to 1 LSB, is defined as

$$H_{\text{avg}} = \frac{\sum_{i=1}^{2^N-2} H(i)}{2^N - 2} \tag{4}$$

where N denotes the ADC resolution. $H(0)$ and $H(2^N - 1)$ are invalid and thus excluded because their input ranges are not doubly bounded. The differential non-linearity (DNL) and integral non-linearity (INL) can be computed by the following equations.

$$DNL(i) = \frac{H(i)}{H_{\text{avg}}} - 1 \quad \text{LSB} \tag{5}$$

$$INL(i) = \begin{cases} 0, & \text{if } i = 0 \\ DNL(i) + INL(i-1), & \text{if } i \neq 0 \end{cases} \tag{6}$$

The linear histogram testing is efficient and only incurs low post-processing efforts. However, direct implementation is impractical because on-chip generation of the required high-resolution ramp is non-trivial and usually causes unacceptable area overhead.

3.2 SAR ADC MCT Testing

The SAR ADC linearity can be estimated by MCT testing [9]. For an N-bit SAR ADC, there are N MCTs, one for each bit. Recall that $\mu_{i,k}$ represents the codes for which the last $i+1$ bits are in the form 2^i. If the SAR ADC has no missing code, the major carrier transition of bit i, denoted by $MCT(i)$, is as follows.

$$\text{MCT}(i) = V_{\text{TL}}(\mu_{i,k}) - V_{\text{TL}}(\mu_{i,k} - 1) \tag{7}$$

$$= V_{\text{CW}}(\mu_{i,k} - 1) \tag{8}$$

where $V_{CW}(x)$ denotes the code width of code x.

Note that MCT (i) appears in the I/O transfer curve for 2^{N-i-1} times because $\left|\hat{\mathcal{M}}_i\right| = 2^{N-i-1}$. Once MCTs are available, the SAR ADC's I/O transfer curve can be constructed for non-linearity analysis.

Definition of MCT is more complicated when there are missing codes. Assuming that there are m_i consecutive missing codes before $\mu_{i,k}$, i.e., codes $\mu_{i,k} - m_i$ to $\mu_{i,k} - 1$ are missing but code $\mu_{i,k} - m_i - 1$ is not, MCT (i) is defined as follows.

$$MCT(i) = V_{\text{TL}}(\mu_{i,k}) - V_{\text{TL}}(\mu_{i,k} - m_i - 1) \tag{9}$$

$$= V_{\text{CW}}(\mu_{i,k} - m_i - 1) \tag{10}$$

Note that, due to missing codes, MCT (i) may appear on the I/O transfer curve for less than 2^{N-i-1} times; this makes it difficult to measure MCT (i) from the ADC I/O transfer curve because there is no telling whether the target code is missing or not.

Consider the example in Fig. 3. For this 10-bit ADC, we have $\hat{\mathcal{M}}_9 = \{\mu_{9,0}\} = \{512\}$. Due to the capacitor mismatch in C_9, there are ten missing codes (from code 502 to 511) in the I/O transfer curve. According to Eqs. 9 and 10, the MCT of bit 9 is

$$\text{MCT}(9) = V_{\text{TL}}(512) - V_{\text{TL}}(501) \tag{11}$$

$$= V_{\text{CW}}(501) \tag{12}$$

Once all the MCTs are measured, the ADC I/O transfer curve can be constructed for DNL and INL analysis. Note that in [9], the authors proposed to directly control the CDAC to generate MCTs, and measure them by a coarse DfT DAC and the comparator. Although effective, the underlying sequential search algorithm may incur long test time. Furthermore, the DfT DAC occupies one input of the comparator; this makes [9] unsuitable for fully-differential designs.

4 MCT-Based SAR ADC Testing and Calibration

4.1 Overview

The basic idea of the proposed technique is to test and calibrate the embedded SAR ADC by extracting the individual bit weights.

Figure 4 shows the proposed testing and calibration flow. It begins with the "bit-weight extraction" loop; the process is from LSB to MSB. In the i-th iteration, MCT (i) is generated and measured. The corresponding bit weight, W_i, is computed from the measured MCT (i) and W_j's for $j < i$. After all the bit weights are extracted, the ADC I/O behavior model can be constructed. By stimulating the modeled ADC with *numerical* linear ramp and sinusoidal wave, the ADC static and dynamic performance, both before and after calibration, can be estimated. Finally, if the post-calibration performance meets the desired

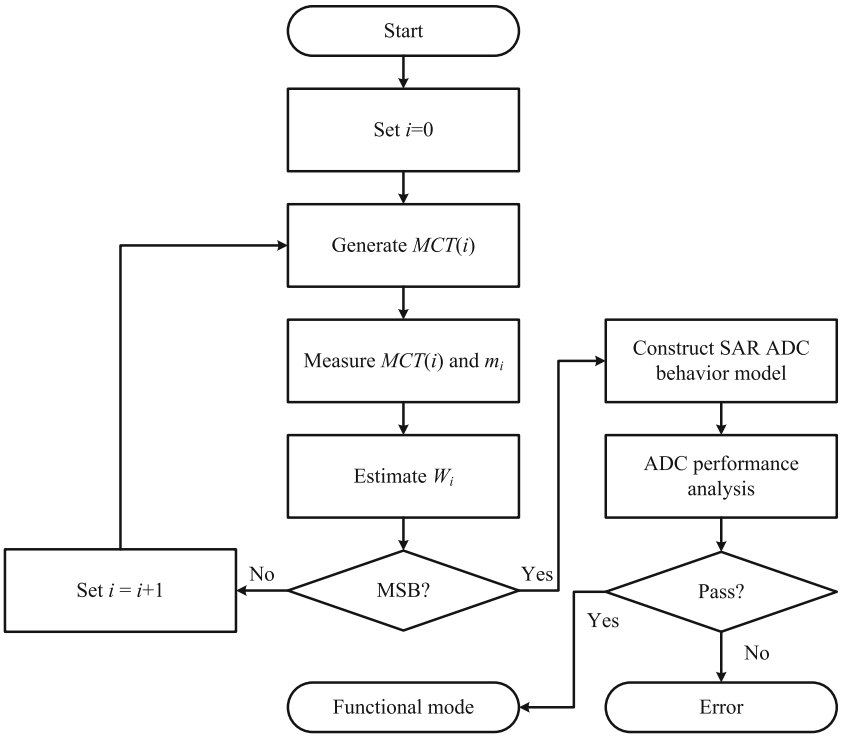

Fig. 4 The proposed testing and calibration flow

specification, the extracted bit weights will be stored and used to calibrate the ADC raw code during functional operation; otherwise, the SAR ADC will be considered failed.

Figure 5 shows the architecture of the proposed SAR ADC testing and calibration technique. In this work, the sub-radix-2 conversion is employed to avoid MDLs; this also reduces the required MCT measurement range because MDLs correspond to large code widths. Modification to the SAR control logic is minimal because the software test/calibration procedures are executed inside the CPU or DSP core. The SAR control logic in Fig. 5 differs from the regular one in that it allows direct external control over the switches via the ***S*** inputs; this suffices to generate the desired MCTs.

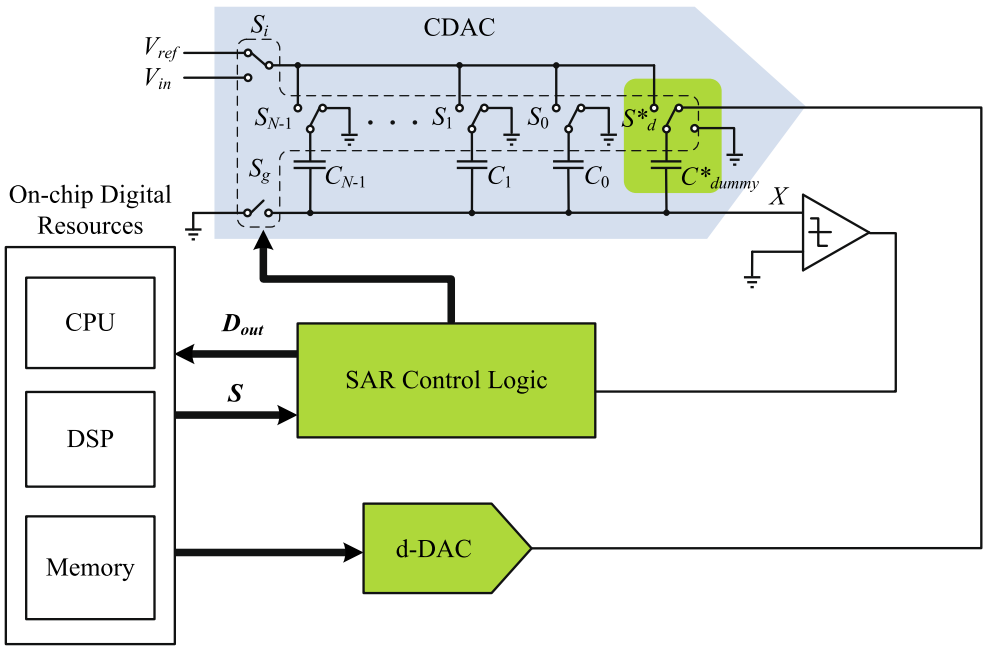

Fig. 5 The proposed self-testing and calibration architecture

The MCTs are measured by the comparator and the d-DAC that couples to the dummy capacitor (C_{dummy}). The full scale range (FSR) of d-DAC is V_{ref}. Coupling the d-DAC to C_{dummy} results in an effective analog measurement range from 0 to $C_{\text{dummy}}/C_{\text{total}} \cdot V_{\text{ref}}$; this allows one to accurately measure the MCTs by a low-resolution d-DAC. In the proposed technique, there is no specific d-DAC test procedure because of its relatively low resolution—five bits in our experiment. Thus, the d-DAC errors are implicitly observed through abnormal testing and calibration outcomes. In practice, one may utilize the SAR ADC (which has much higher resolution) to validate the d-DAC in advance. Note that, to cover all possible MCT values, the size of C_{dummy} should be slightly larger than the unit capacitor C_0. Unlike [9], the proposed technique leaves the comparator's negative input untouched; this makes it suitable for the differential SAR ADC.

The extract bit weights may be stored in volatile or non-volatile memory depending on whether the calibration process is to be executed just one time during manufacturing testing or routinely, e.g., after each power-up. Based on the extracted bit weights, the software test procedure can assess the post-calibration performance to make the pass/fail decision. During the functional mode, a software calibration procedure receives the raw ADC output and computes the calibrated output.

4.2 MCT Generation

MCTs can be generated by properly switching the capacitors in the CDAC; the process is very similar to the SAR A/D conversion. Consider the SAR ADC in Fig. 5, $MCT(i)$ can be generated as follows.

1. Close S_g, connect the top plate of C_i to V_{ref}, and the top plates of all the other capacitors to ground.
2. Open S_g and then connect all the capacitor top plates to ground. V_X becomes

$$V_X = -\frac{C_i}{C_{\text{total}}} \cdot V_{\text{ref}} \tag{13}$$

$$= -V_{\text{TL}}\left(2^i\right) \tag{14}$$

3. Perform the primitive SAR operation using less significant capacitors (C_{i-1} to C_0). The obtained raw code will be $2^i - 1 - m_i$ and V_X will become

$$V_X = -V_{\text{TL}}\left(2^i\right) + V_{\text{TL}}\left(2^i - 1 - m_i\right) = -\text{MCT}\,(i) \tag{15}$$

This can be illustrated by the example shown in Fig. 3. If we charge V_X to $-V_{\text{TL}}(512)$ by steps 1 and 2, and then perform the SAR operation; the obtained ADC raw code will be 501 and V_X will become $-V_{\text{TL}}(512) + V_{\text{TL}}(501) = -MCT(9)$.

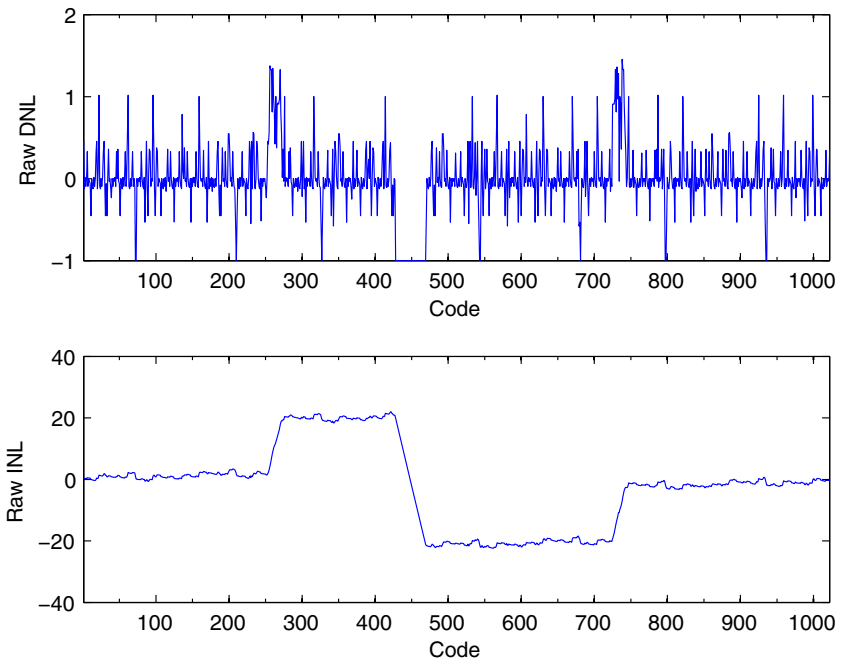

Fig. 6 DNL and INL before calibration

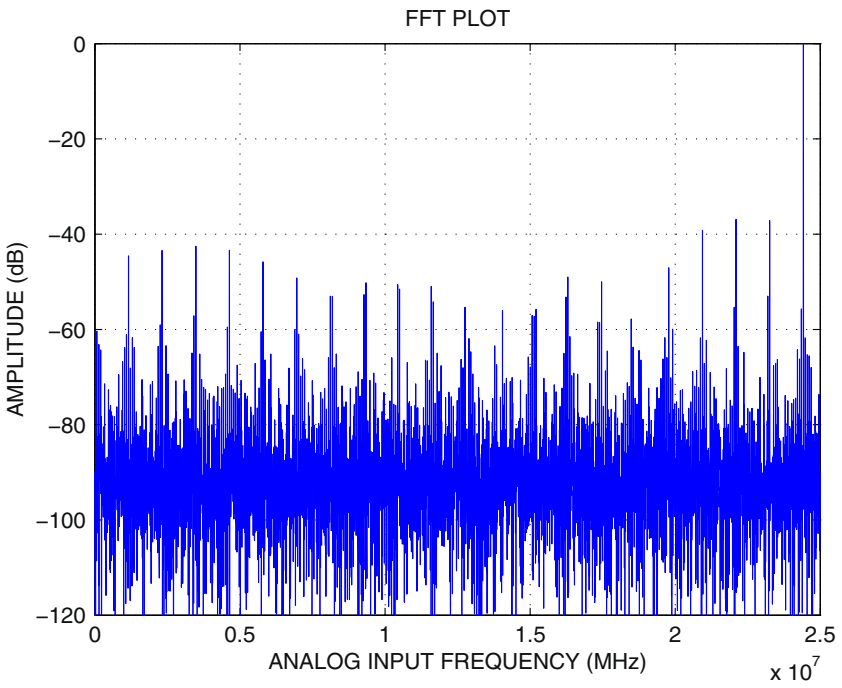

Fig. 7 Frequency spectrum before calibration

Recall that, due to missing codes, not all MCT (i)'s appear on the SAR ADC I/O transfer curve. In the proposed technique, the first MCT (i) (that corresponds to $\mu_{i,0} = 2^i$) is measured even though it may not appear in the ADC transfer curve; this is possible by skipping the SAR operations prior to bit i in the MCT generation procedure.

4.3 MCT Measurement

The generated MCTs are measured by the comparator and the d-DAC. The output dynamic range of d-DAC is set from 0 to V_{ref}; coupling the d-DAC to C_{dummy} (after MCT generation) results in an effective analog measurement range from 0 to $C_{\text{dummy}}/C_{\text{total}} \cdot V_{\text{ref}}$. Let

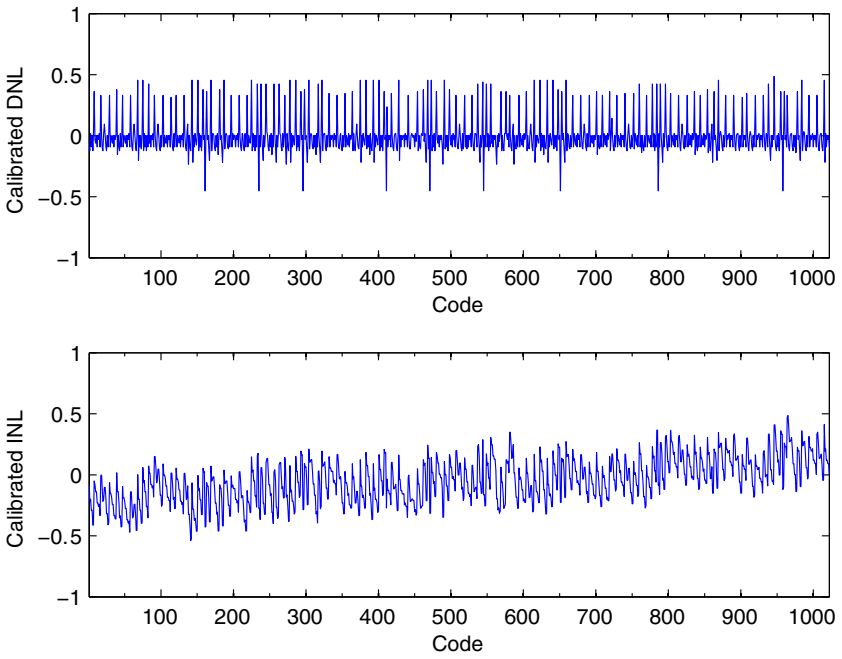

Fig. 8 DNL and INL after calibration

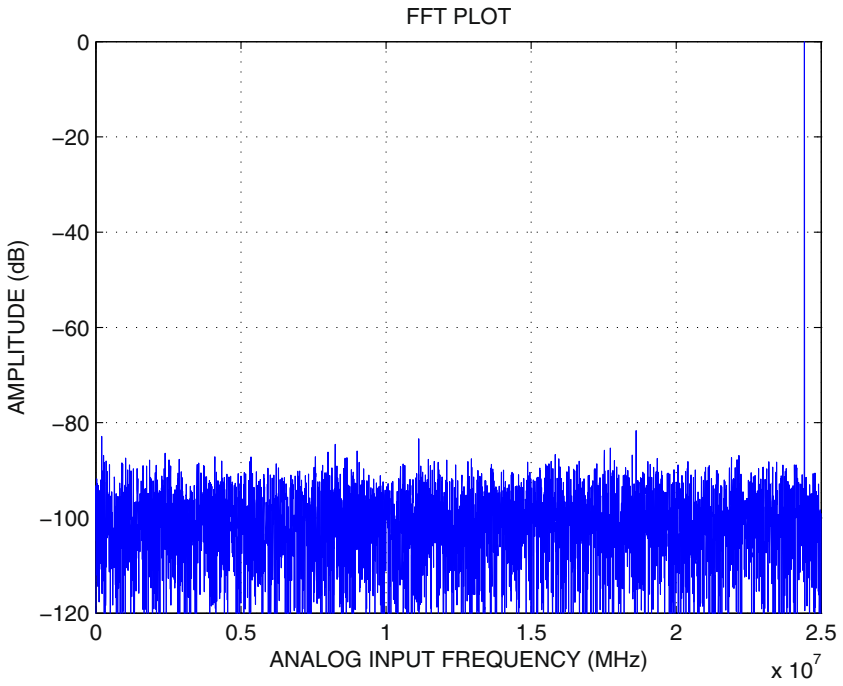

Fig. 9 Frequency spectrum after calibration

R be the d-DAC resolution and $B_{\text{in}} = b_{R-1} \ldots b_1 b_0$ the d-DAC input code. Increasing B_{in} by 1 will raise V_X by

$$\Delta_{d-DAC} = \frac{1}{2^R - 1} \cdot \frac{C_{\text{dummy}}}{C_{\text{total}}} \cdot V_{\text{ref}} \tag{16}$$

where Δ_{d-DAC} denotes the effective step size of d-DAC during MCT measurement. With the d-DAC, the $MCT(i)$ measurement flow is as follows.

1. Connect the top plate of C_{dummy} to the d-DAC output and set $B_{\text{in}} = 0$. Here, V_X remains $-MCT(i)$.
2. Set k to $R - 1$.
3. Set b_k to 1, charge redistribution forces V_X to become

$$V_X = -MCT(i) + B_{\text{in}} \cdot \Delta_{d-DAC} \tag{17}$$

4. If $V_X > 0$, reset b_k to 0.
5. If $k > 0$, set $k = k - 1$ and go to 3; otherwise, go to 6.
6. Let $\beta(i)$ denote the measured value of $MCT(i)$, we have $\beta(i) = B_{\text{in}} + 1$.

The MCT measurement process is also based on SAR operation; this further reduces the test time from $O\left(2^R\right)$ in [9] to $O(R)$ and facilitates the noise removal process which will be introduced later.

4.4 Bit-Weight Extraction

The individual bit weights of the SAR ADC can be computed from the measured MCTs. First, Eq. 15 can be re-written as follows.

$$V_{\text{TL}}\left(2^i\right) = V_{\text{TL}}\left(2^i - m_i - 1\right) + \text{MCT}\,(i) \tag{18}$$

If we normalize all the terms in Eq. 18 to Δ_{d-DAC}, the MCT measurement resolution, we can replace $V_{\text{TL}}\left(2^i\right)$ by W_i, $V_{\text{TL}}\left(2^i - m - 1\right)$ by the sum of weights of non-zero bits in $2^i - m_i - 1$, and MCT (i) by $\beta\,(i)$.

Table 1 Capacitor weights ($W_i / W_{\text{total}} \cdot 100\ \%$)

Bit	Actual value (%)	Estimated value (%)	Estimation error (%)
11	43.8569	43.8653	−0.0192
10	26.7263	26.7295	−0.0120
9	13.5355	13.5407	−0.0384
8	7.2372	7.2345	0.0373
7	3.9884	3.9912	−0.0702
6	2.2343	2.2321	0.0985
5	1.1136	1.1087	0.4400
4	0.6431	0.6356	1.1662
3	0.3261	0.3282	−0.6440
2	0.1867	0.1863	0.2142
1	0.0982	0.0976	0.6110
0	0.0535	0.0503	5.9813

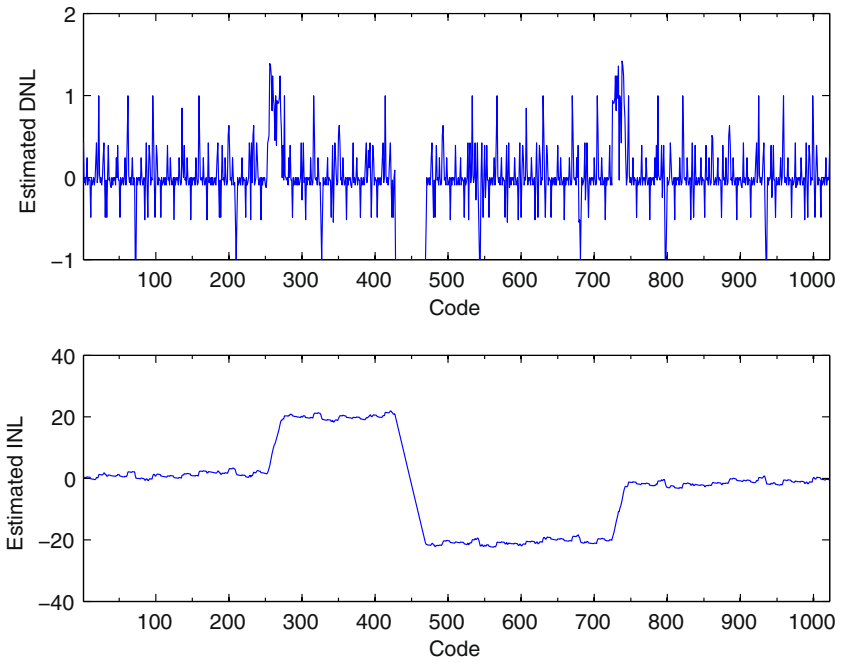

Fig. 10 Estimated DNL and INL before calibration

Let $Z_i = z_{N-1}z_{N-2}\cdots z_1 z_0$ be the ADC code obtained at the end of $MCT(i)$ generation, i.e., $Z_i = 2^i - m_i - 1$. W_i can be derived according to Eq. 19.

$$W_i = \begin{cases} \beta(i) & \text{if } i = 0 \\ \beta(i) + \sum_{j=0}^{i-1} z_j \cdot W_j & \text{if } i > 0 \end{cases} \tag{19}$$

4.5 SAR ADC Calibration

Let $D = d_{N-1}d_{N-2}\ldots d_0$ be the (un-calibrated) raw ADC output and M the target ADC resolution (typically, $M < N$). Once the bit weights are available, in the

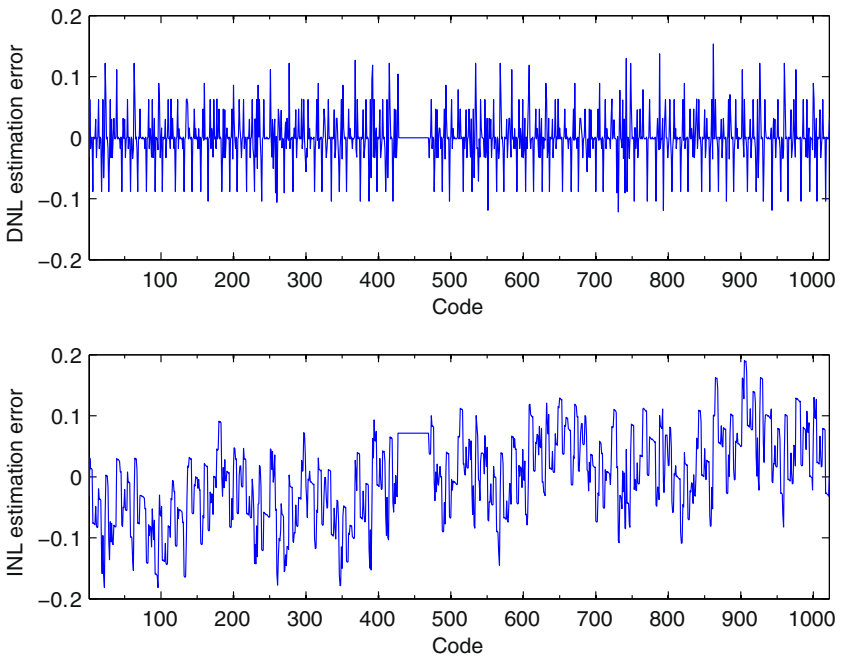

Fig. 11 Estimation error of DNL and INL before calibration

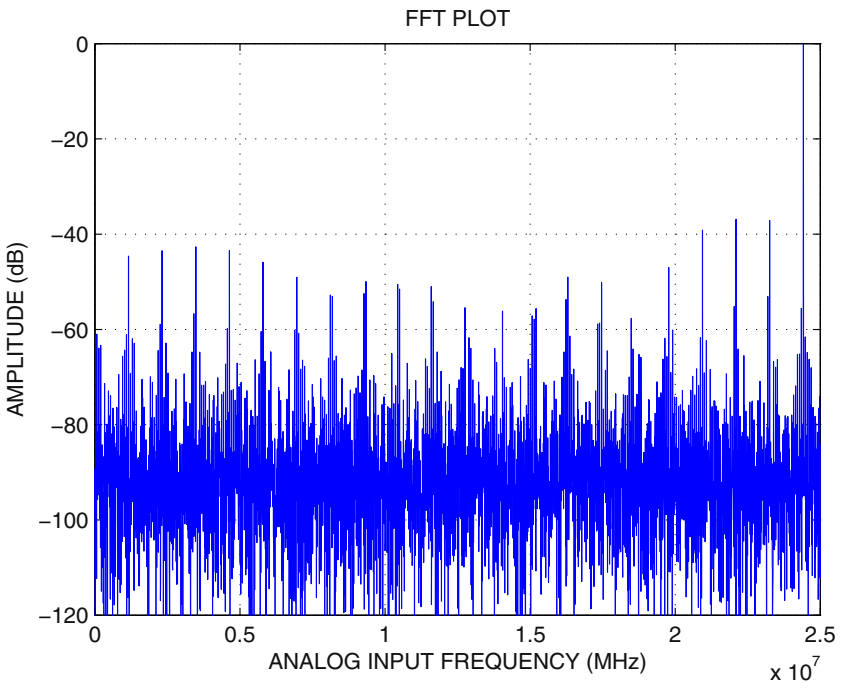

Fig. 12 Estimated frequency spectrum before calibration

function mode, the calibrated output D^* can be computed according to Eq. 20 in which $W_{\text{total}} = \sum_{i=0}^{N-1} W_i$.

$$D^* = \frac{\sum_{i=0}^{N-1} W_i \cdot d_i}{W_{\text{total}}} \cdot \left(2^M - 1\right) \tag{20}$$

Note that the value associated with the raw code is $\sum_{i=0}^{N-1} 2^i \cdot d_i$. In Eq. 20, we (1) replaced the ideal bit weight 2^i with the extracted bit weight W_i, (2) normalized the resulting sum of weights, $\sum_{i=0}^{N-1} W_i \cdot d_i$ to W_{total}, and (3) multiply the normalized value (which ranges from 0 to 1) by $2^M - 1$ to realize the desired resolution.

4.6 SAR ADC Performance Analysis

Using the extracted bit weights, the SAR ADC behavior model can be constructed. To estimate the DNL/INL performance, the software test procedure stimulates the ADC model with *numerical* linear ramp

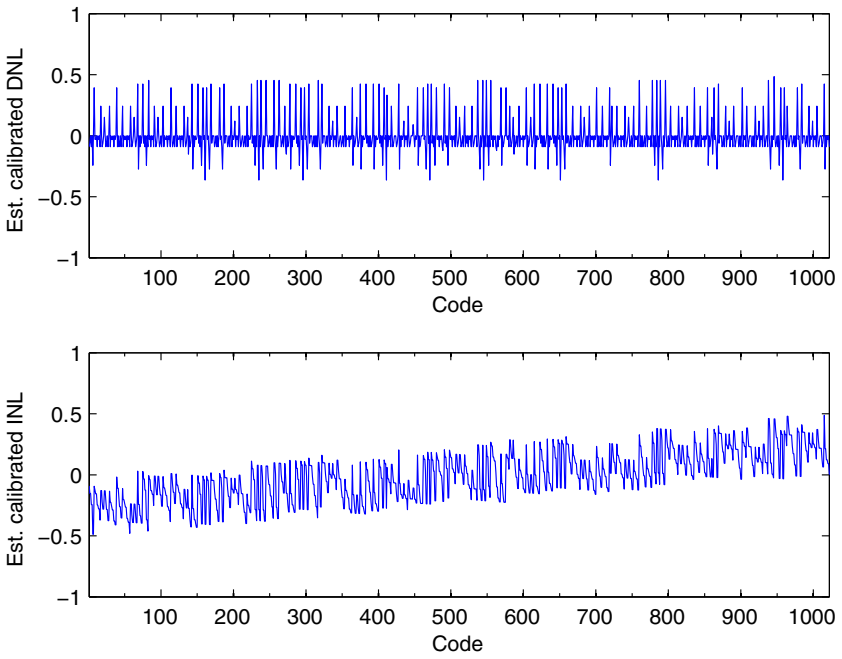

Fig. 13 Estimated DNL and INL after calibration

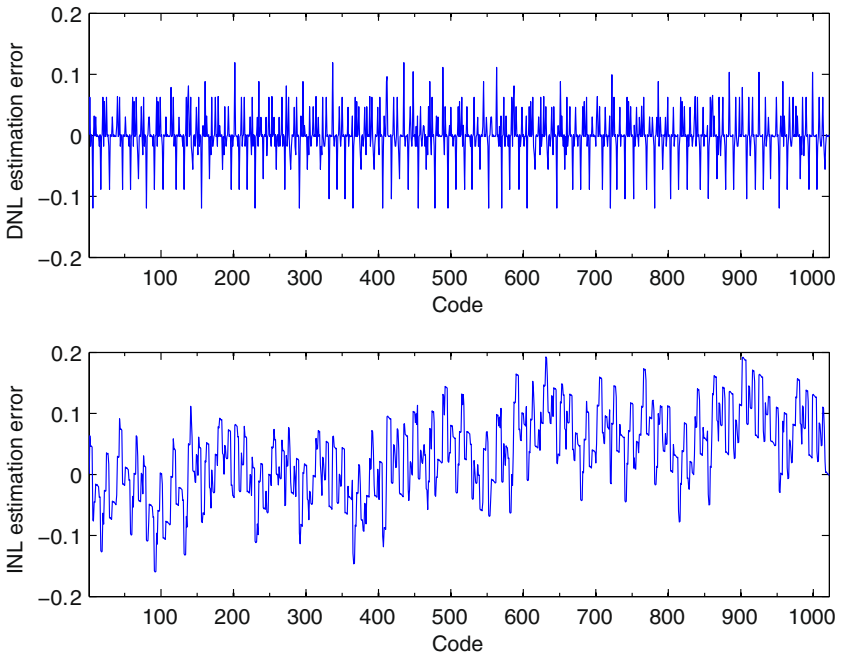

Fig. 14 Estimation error of DNL and INL after calibration

and perform histogram analysis. The dynamic performance, e.g., ENOB, of the ADC, is derived in a similar manner. A *numerical* sinusoidal signal is applied to the constructed model and spectrum analysis is performed to analyze the output response.

Note that this works focuses on the capacitor mismatch induced errors. In reality, non-idealities due to switches and comparators will further deteriorate the ADC performance. Thus, the estimated static and dynamic performance is the upper bound of the actual performance.

4.7 Discussion

4.7.1 Noise Effect Removal

The intrinsic noise of the SAR ADC may deteriorate the accuracy of the proposed bit-weight extraction

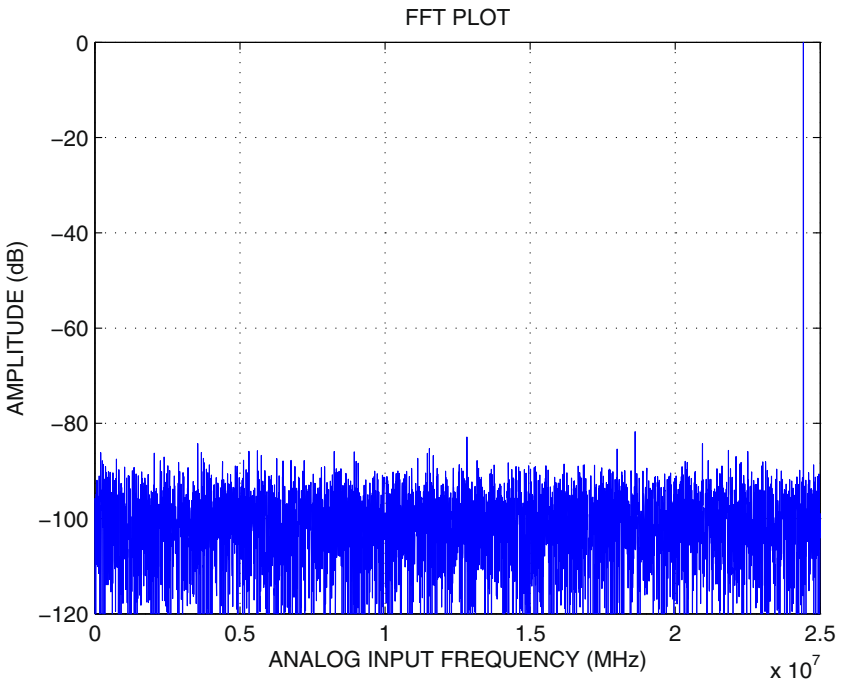

Fig. 15 Estimated frequency spectrum after calibration

Table 2 Simulation results

	Uncalibrated (actual)	Uncalibrated (estimated)	Calibrated (actual)	Calibrated (estimated)
DNL (LSB)	1.45	1.42	0.49	0.48
INL (LSB)	−22.37	−22.37	−0.54	−0.49
SNDR (dB)	30.42	30.42	60.75	60.89
ENOB (Bit)	4.76	4.76	9.80	9.82

process, and thus lowers the achievable test resolution and calibration performance. To eliminate the noise effect, several comparisons are performed for each bit decision of the comparator; the final result is determined by the majority value.

4.7.2 Comparator Resolution

The proposed MCT measurement process requires the comparator to have higher resolution than in the normal operational mode. However, designing the comparator to meet the MCT measurement accuracy at normal operational speed may cause significant increment to the circuit design complexity and power consumption. One possible solution, as indicated by [17], is to increase the comparator resolution by lengthening the comparison time; the cost is longer test time.

4.7.3 Comparator Offset

Another performance limiter of the proposed technique is the comparator offset; it may cause errors to the MCT generation and measurement, and thus degrades the accuracy of the bit-weight extraction process. It is desired that the comparator offset can be calibrated before applying the proposed technique. To remove the comparator offset, [1] employs a DAC to adjust the bulk voltages of the differential pair in the comparator. By increasing the resolution of the DAC, it is possible to suppress the comparator offset to be within 0.1 LSB at 10-bit level [19].

4.7.4 Test Time Analysis

The incurred test time consists of (1) the test application time, and (2) the post-processing time. In the proposed technique, the test application time for each bit is three cycles for MCT generation and at most R (the d-DAC resolution) cycles for MCT measurement. Thus, for an N-bit SAR ADC, the worst case test application time is $N \cdot (3 + R)$ cycles. The post-processing time includes bit weight computation and post-calibration performance analysis. The former is straightforward; the latter, however, is computation and control intensive. The post-processing time strongly depends on the on-chip digital processing power and capacity; hence, detailed analysis is not attempted in this paper.

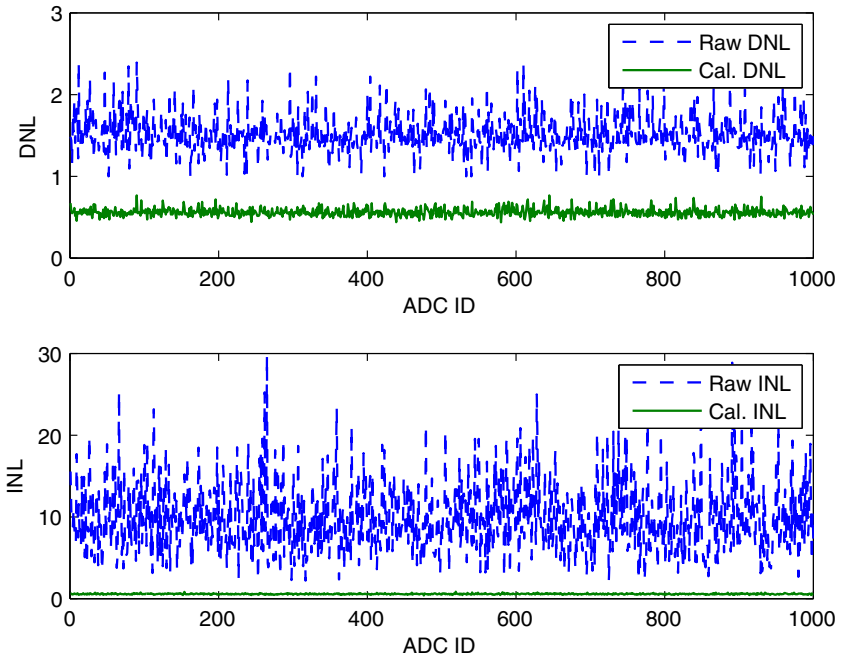

Fig. 16 Peak DNL and INL of 1,000 SAR ADCs

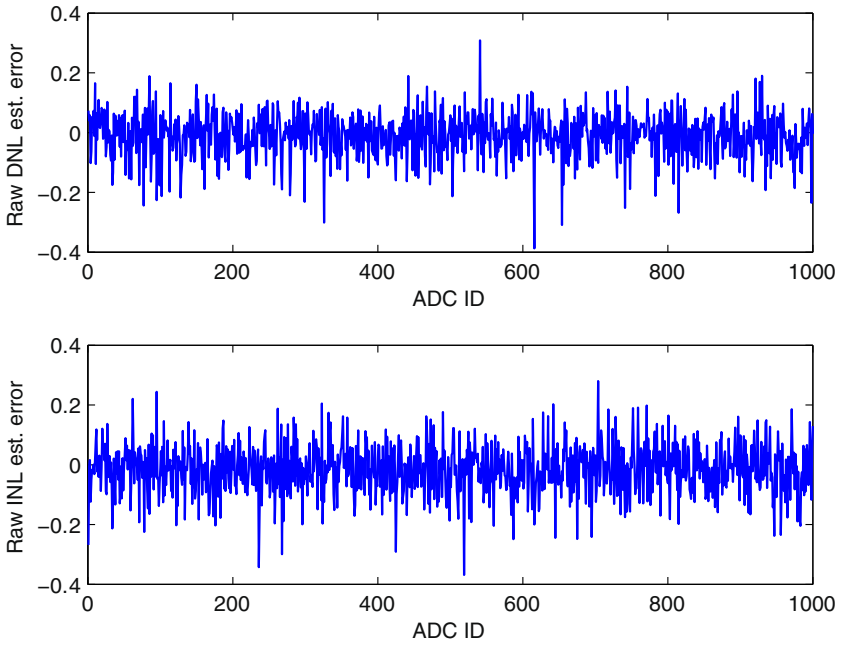

Fig. 17 Maximum DNL/INL estimation error before calibration

5 Simulation Results

Behavior-level numerical simulations using MATLAB are performed to validate the proposed testing and calibration techniques. The simulation setup is as follows.

- The validation vehicle is a 50 MS/s 10-bit SAR ADC with 1 V FSR. The conversion radix (α) is set to 1.85 to avoid MDLs and two redundant bits are added to achieve the desired 10-bit resolution, i.e., the raw ADC output is 12 bits for each A/D conversion.
- For each capacitor, the associated mismatch is a Gaussian distribution; the standard deviation is 3 % of its nominal value.
- The comparator offset is assumed to be calibrated within 0.1 LSB at 10-bit level.
- C_{dummy} is set to $2 \cdot C_0$ to cover all possible MCT values and the DfT DAC (d-DAC) resolution is five bits.

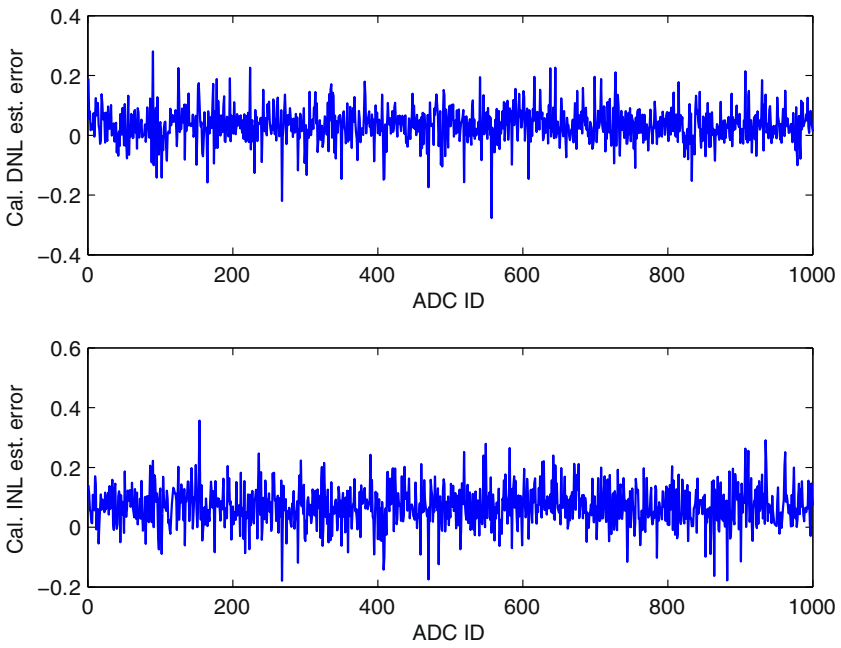

Fig. 18 Maximum DNL/INL estimation error after calibration

– The intrinsic noise of the SAR ADC is also a Gaussian distribution; the standard deviation is set to 0.5 LSB at 10-bit level. To average out the noise effect during testing, each comparator bit decision is determined by the majority value of 63 comparisons.

5.1 ADC Performance Before Calibration

Before applying the proposed testing technique, the 12-bit ADC raw codes are converted to 10-bit ones according to Eq. 20 based on the nominal bit weights, i.e., $C_i = 1.85^i \cdot C_0$.

The DNL and INL before calibration are measured by the noise-free linear histogram testing; the average code hits is 64. Figure 6 shows the DNL (top) and INL (bottom) plots; the peak DNL and INL are 1.45 and −22.37 LSB, respectively.

Then, to measure the effective number of bits (ENOB), we stimulate the ADC with a near Nyquist frequency sinusoidal wave and take 8192 samples at the ADC output. Figure 7 shows the output frequency spectrum of the un-calibrated ADC. The SNDR (signal to noise and distortion ration) is 30.42 dB, and the ENOB is 4.76 bits.

5.2 ADC Performance After Calibration

After applying the proposed testing technique, the extracted bit weights can be used to calibrate the 12-bit ADC raw codes. Figure 8 shows the DNL (top) and INL (bottom) after calibration; the peak DNL and INL are greatly reduced to 0.49 and −0.54 LSB, respectively. The output frequency spectrum after calibration is depicted in Fig. 9, it shows significant noise reduction. The SNDR is improved to 60.75 dB, and the ENOB is increased to 9.80 bits. These results demonstrate the effectiveness of the proposed calibration technique.

5.3 Simulation for the Proposed Testing Technique

In this work, the individual bit weights are extracted by MCT testing; the results can be used for estimating the ADC performance both before and after calibration. Note that this is realized by a software procedure that applies *numerical* test stimulus to the *constructed ADC model*.

5.3.1 Bit-Weight Extraction

Table 1 shows the bit weight extraction results. In this table, column 1 lists the bit number; columns 2 and 3 show the normalized actual and estimated bit weights ($W_i / W_{\text{total}} \cdot 100\ \%$); finally, column 4 shows the estimation error. It should be noted that, in this example, the comparator offset is 0.09 LSB at 10-bit level.

As shown in column 4, the largest estimation error occurs at the LSB; it is because the LSB weight is very small and thus is more sensitive to the comparator offset during measurement. On the other hand, the estimation errors for the upper half bits (bit 11 to 6) are

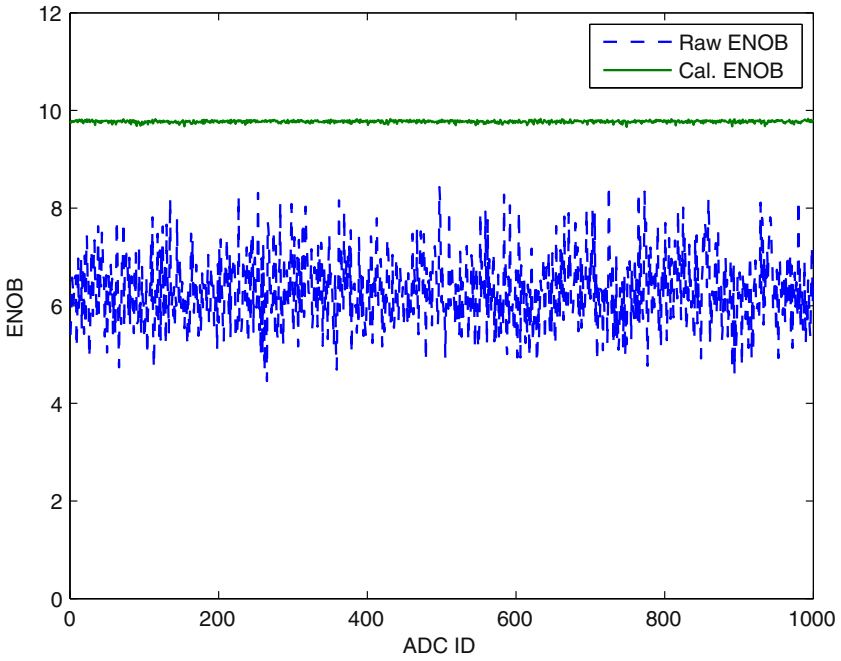

Fig. 19 ENOB of 1,000 SAR ADCs

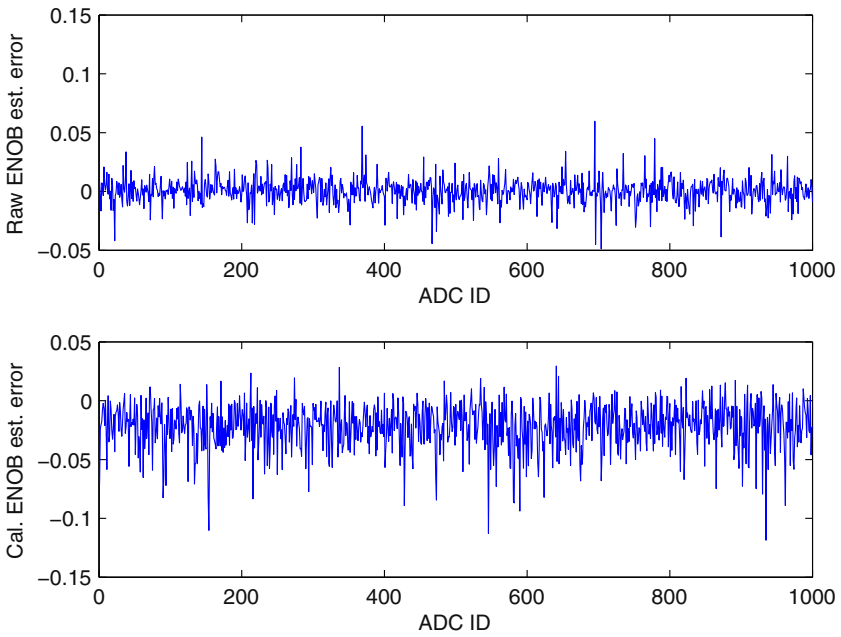

Fig. 20 ENOB estimation error of 1,000 SAR ADCs

all less than 0.1 %; this provides precision estimation of the ADC performance.

5.3.2 Pre-Calibration Performance Analysis

Figure 10 shows the estimated DNL (top) and INL (bottom) before calibration; the peak DNL and INL are 1.42 and −22.37 LSB, respectively. These results are almost identical to Fig. 6. The estimation errors are shown in Fig. 11; they are all below 0.2 LSB. Figure 12 shows the estimated output frequency spectrum before calibration; the SNDR is 30.42 dB and the ENOB is 4.76-bit.

5.3.3 Post-Calibration Performance Estimation

Figure 13 shows the estimated DNL (top) and INL (bottom) after calibration; the peak DNL and INL are 0.48 and −0.49 LSB, respectively. The estimation errors are shown in Fig. 14; they are all below 0.2 LSB. The estimated output frequency spectrum after calibration is depicted in Fig. 15. The SNDR is 60.89 dB, and the ENOB is 9.82-bit.

5.3.4 Summary

Table 2 summarizes the simulation results. In this table, column 1 lists the performance metrics: DNL, INL, SNDR, and ENOB. Columns 2 and 3 show the actual and estimated performance of the un-calibrated ADC, respectively; columns 4 and 5 are those of the calibrated ADC. Apparently, all the estimated results are very close to their actual values; this demonstrates the effectiveness of the proposed testing technique.

5.4 Massive Simulation

To further validate our work, we apply the proposed technique to test and calibrate 1,000 randomly perturbed SAR ADCs; these instances are generated using the aforementioned simulation setup. Figure 16 depicts the absolute peak DNL and INL of each case; the dashed and solid line show the results before and after calibration, respectively. With the proposed calibration technique, the average peak DNL/INL are significantly improved from 1.51/9.87 LSB to 0.56/0.57 LSB. The maximum estimation errors before and after calibration are shown in Figs. 17 and 18; they are all within 0.39 LSB.

Figure 19 depicts the ENOB before (dashed line) and after (solid line) calibration; the average ENOB is improved from 6.31-bit to 9.77-bit. Figure 20 shows the ENOB estimation errors before (top) and after (bottom) calibration; they are all less than 0.15-bit. These results demonstrate the robustness of the proposed technique.

6 Conclusion

This paper presents a simple yet efficient testing and calibration technique for the SAR ADC. Utilizing MCT testing, the individual bit weights are extracted. From the results, the non-ideal ADC I/O behavior can

be calibrated and the performance both before and after calibration can be accurately estimated. Simulation results validate the effectiveness and robustness of the proposed technique.

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