Timing analysis / pipelining

V1.0

- Overview of timing report generated by Vivado
- How pipelining can improve you timings
- Workshop

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Report file - check_timing_report

- *_timing.rpt
- check_timing report → error report

```
Table of Contents
-----------------
1. checking no clock (0)
2. checking constant clock (0)
3. checking pulse width clock (0)
4. checking unconstrained internal endpoints (0)
5. checking no input delay (8)
6. checking no output delay (4)
7. checking multiple clock (0)
8. checking generated clocks (0)
9. checking loops (0)
10. checking partial input delay (0)
11. checking partial output delay (0)
12. checking latch loops (0)
```

Can be ignored most of the time

Report file - Design Timing Summary

- WNS → Worst Negative Setup slack
- WHS → Worst Hold Slack
- WNS and WHS must be greater than or equal to zero

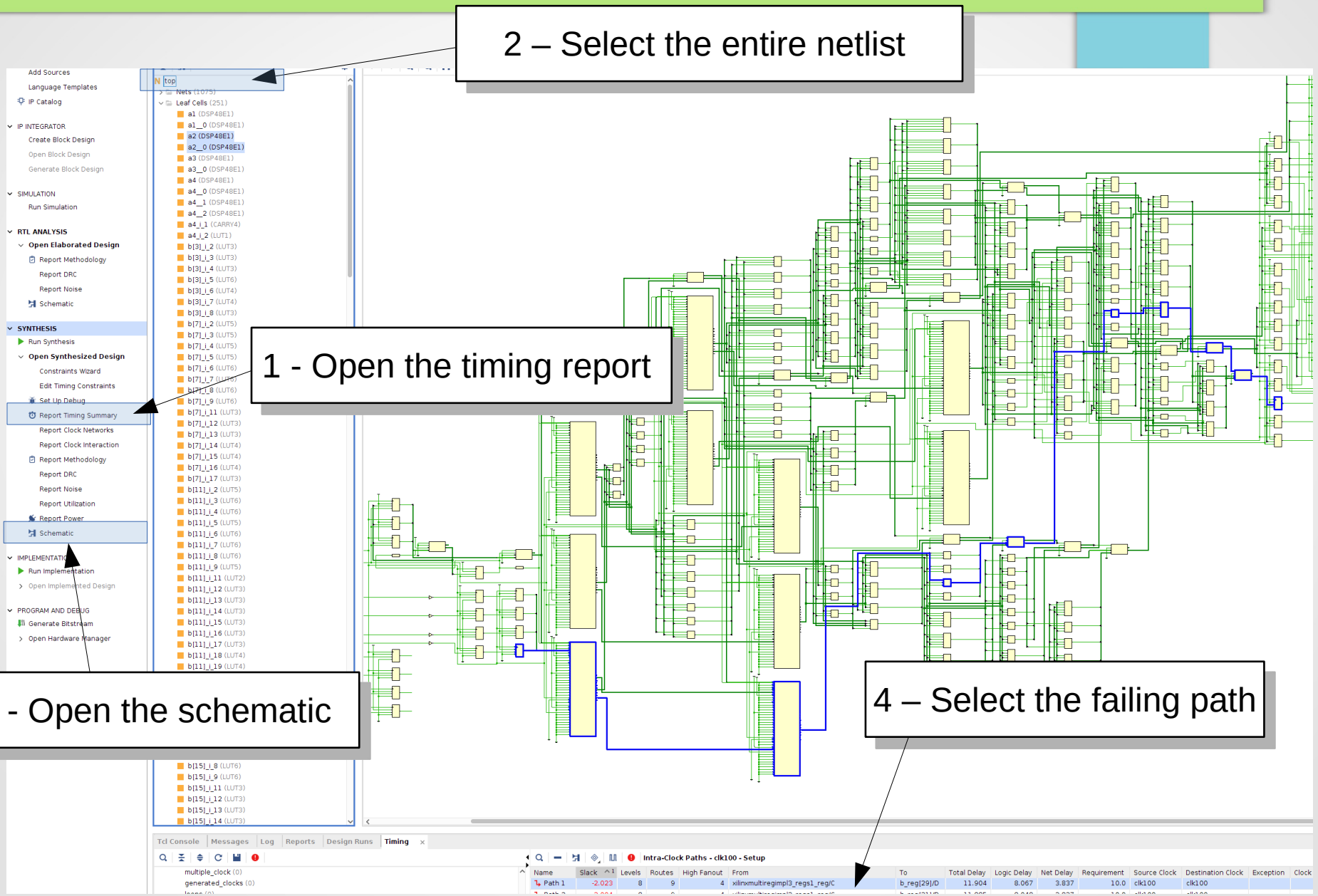
WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	...
-0.755	-4.588	10	146	0.263	0.000	...

Most influenced by your design

Report file - Max Delay Paths

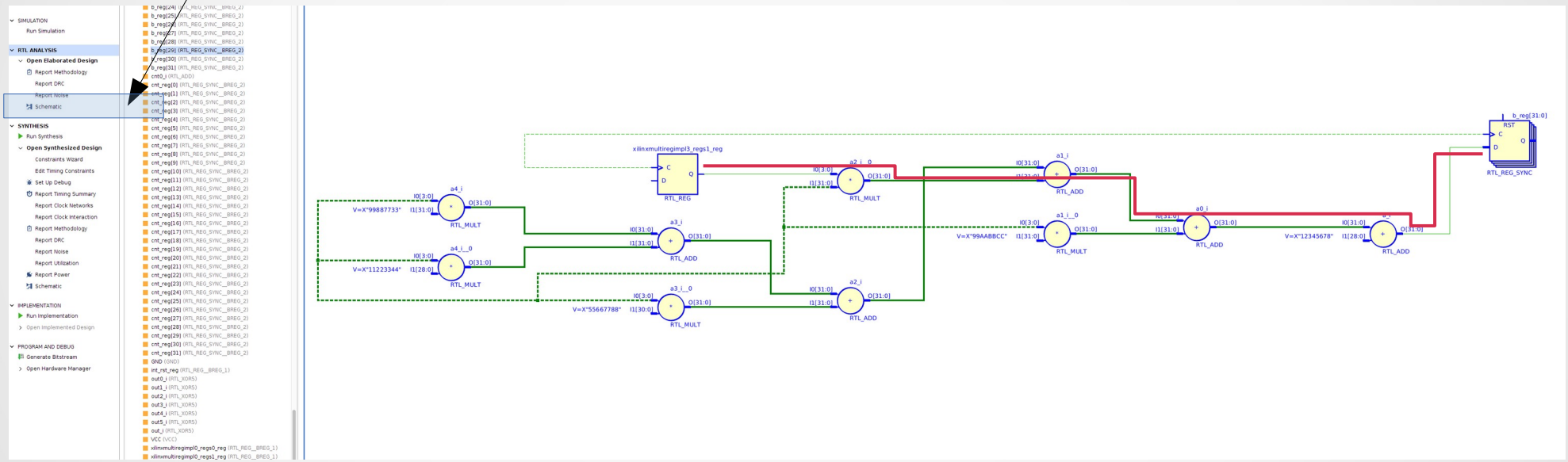
```
    Max Delay Paths
--------------------------------------------------------------------------------
Slack (VIOLATED) :        -0.755ns  (required time - arrival time)
  Source:                 xilinxmultiregimpl0_regs1_reg/C
                            (rising edge-triggered cell FDRE clocked by clk100
  Destination:            b_reg[29]/D
                            (rising edge-triggered cell FDRE clocked by clk100
  Path Group:             clk100
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk100 rise@10.000ns - clk100 rise@0.000ns)
  Data Path Delay:        10.790ns  (logic 7.724ns (71.586%)  route 3.066ns (28.414%))
  Logic Levels:           7  (CARRY4=3 DSP48E1=2 LUT3=1 LUT6=1)
  Clock Path Skew:        -0.039ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.795ns = ( 14.795 - 10.000 )
    Source Clock Delay      (SCD):    5.093ns
    Clock Pessimism Removal (CPR):    0.259ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

Visual inspection



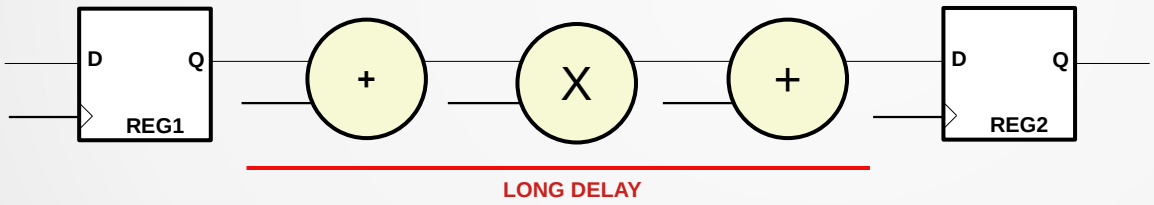
Visual inspection

Open the elaborated schematic



Pipelining

- Long combinatorial path can be *cut* into smallest chunks
- We insert registers to *cut* combinatorial path
- Latency is introduced



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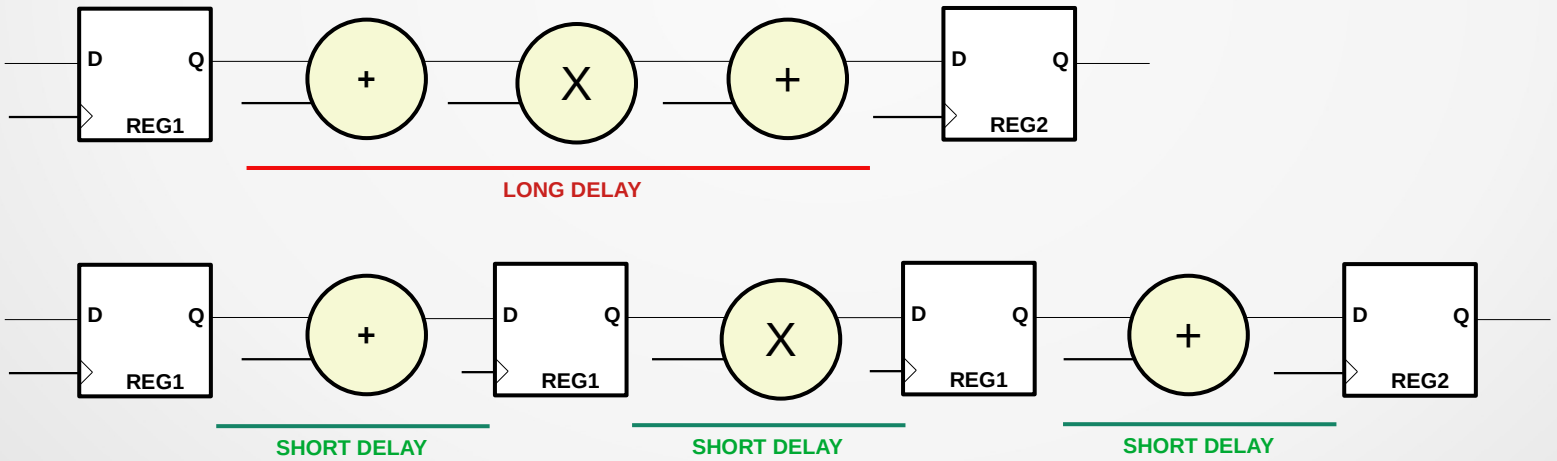

Workshop - extra0

- Build the non pipelined version of workshop_extra0
- Look at the timing report, open Vivado and look at the RTL schematics
- Design the pipelined version of workshop_extra0
- Make sure it works :)
- Look at the timing report, open Vivado and look at the RTL schematics